Docket No.: MAS-FIN-141

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MAIL STOP: APPEAL BRIEF-PATENTS

By: _____ Date: September 15, 2003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

Applicant : Robert-Christian Hagen et al.

Applic. No.: 09/993,266

Filed : November 19, 2001

Title : Electronic Component with Shielding and Method for its Production

Examiner : Dana Farahani - Art Unit: 2814

BRIEF ON APPEAL

Hon. Commissioner for Patents,

S i r :

This is an appeal from the final rejection in the Office Action dated March 11, 2003, finally rejecting claims 1-12.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $320.00 to cover the fee for filing the *Brief on Appeal*.

Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1-12 are rejected and are under appeal. Claims 13-28 are withdrawn from further consideration.

Status of Amendments:

No claims were amended after the final Office Action. *A Response under 37 CFR § 1.116* was filed on June 13, 2003. The Supervisory Primary Examiner stated in an *Advisory Action* dated July 1, 2003, that the request for reconsideration had been considered but did not place the application in condition for allowance.

Summary of the Invention:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention

relates to an electronic component with shielding and to a method for its production.

Appellants explained on page 21 of the specification, line 10, that, referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown a schematic cross section view of an electronic component 1 with shielding 2 according to a first embodiment of the invention. In Fig. 1, the reference number 3 designates a semiconductor chip. The reference number 4 designates a semiconductor substrate with an active upper side 5 and a passive rear side 6. The substrate 4 is part of a wafer 13. The reference number 7 designates an electrically conductive buried layer in a region of the rear side 6 of the semiconductor substrate 4 and the reference number 8 designates a contact area on the active upper side 5 of the semiconductor chip 4, which is provided for a connection to an external ground potential terminal 9. The reference number 10 designates a ground lead within the semiconductor substrate 4 and the reference number 11 designates an electrically conductive annular layer within the semiconductor substrate 4, which may serve as the ground lead 10 for the connection between the contact area 8 and the buried layer 7.

Appellants outlined on page 22 of the specification, line 4, that the electronic component 1 with the shielding 2 of Fig. 1 has the semiconductor chip 3 with the active upper side 5 and the passive rear side 6. In the region of the passive rear side 6 there is within the semiconductor substrate 4 an electrically conductive buried layer with an impurity concentration of at least 1×10^{20} cm^{-3}, which on account of the high impurity concentration has virtually metallically conductive properties. The upper side 5 has at least one contact area 8, which is connected to the ground potential terminal 9. The electrically conductive buried layer 7 is connected to the contact area 8 on the upper side 5 via the electrically conductive ground connection 10 within the semiconductor substrate 4. The ground connection 10 is a region which reaches from the contact area 8 to the buried layer 7 and has an impurity concentration of at least 1×10^{20} cm^{-3}, and is consequently virtually metallically conductive. Via the ground connection 10 within the semiconductor substrate 4, the external ground potential 9 is connected to the buried layer 7.

Appellants further outlined on page 22 of the specification, line 24, that, with the rear-side shielding by the buried layer 7, it is possible to protect the active upper side 5 with its active integrated circuit from electromagnetic

interference fields. All that is required for this purpose is at least one ground lead within the semiconductor substrate 4. A ground lead of this type can be achieved by deep diffusion of impurities, for example into a silicon substrate.

Appellants described on page 23 of the specification, line 7, that, in the exemplary embodiment according to Fig. 1, the buried layer 7, highly doped with an impurity concentration of at least 1×10^{20} cm^{-3}, was achieved by ion implantation from the rear side. For this purpose, the semiconductor wafer 13, which in this exemplary embodiment is formed of a monocrystalline silicon slice, was polished on both sides, with the result that a polished surface was prepared as the rear side 6 for ion implantation and the other polished surface was provided as the upper side 5 for corresponding structuring with the electronic components. According to the embodiment as shown in Fig. 1, the electronic component 1 is structured in such a way that, with its buried layer 7 as shielding and the ground connection 10 to the upper side, it is configured for a flip-chip mounting technique. For this purpose, it has on the contact areas 8 of the upper side 5 solder contact bumps 20, which are suitable for placing directly onto a printed-circuit board 14 or a ceramic substrate 15. Consequently, the entire rear side of the

semiconductor chip 3 forms an effective shielding for protection of the upper side 5 of the semiconductor chip 3 fitted with active components.

Appellants outlined on page 24 of the specification, line 4, that Fig. 2 shows a schematic cross section of the electronic component 1 with the shielding 2 according to a second embodiment of the invention. Components of Fig. 2, which perform the same functions as in Fig. 1 are identified by the same reference numerals.

It is also outlined on page 24 of the specification, line 10, that, in the case of the embodiment according to Fig. 3, the semiconductor chip, which can be seen in Fig. 1 has been soldered with its solder contact bumps on output contact areas 18 of a multi-layer printed-circuit board. The buried layer 7 was produced for this embodiment of the invention by epitaxial growth of an epitaxial layer, highly doped with at least an impurity concentration of 1×10^{20} cm^{-3}, on a base substrate with a subsequent epitaxial layer which has only intrinsic conductivity. In the example of Fig. 2, the base substrate was ground down until thin, with the result that only a slight residue on the rear side above the buried layer remains visible in cross section.

It is stated in the last paragraph on page 24 of the specification, line 23, that, introduced from the active upper side 5 into the regions of the intrinsically conductive monocrystalline silicon lying above the buried layer is the integrated circuit, which is surrounded by a ring of highly doped silicon material. The annular layer 11 has an impurity concentration of at least 1×10^{20} cm^{-3}, and consequently has virtually metallic conductivity. In the case of the embodiment of Fig. 2, the semiconductor chip 3 which can be seen in Fig. 1 has been soldered with its solder contact bumps onto the output contact areas 18 of a multi-layer printed-circuit board.

Appellants explained on page 25 of the specification, line 8, that an intermediate space between the active upper side 5 of the semiconductor chip 3 is filled by a plastic molding compound 23. Side edges 24 and 25 of the plastic molding compound can, if need be, cover the entire semiconductor chip 3 and its side edges and, if required, can also be spread over the rear side 6 with the buried layer 7. This depends on the area of application of the electronic component shown in Fig. 2.

Appellants further outlined on page 25 of the specification, lien 16, that, in Fig. 2, the multi-layer printed-circuit

board 14 is surrounded by a ground-carrying line 22 and connected to ground potential 9, with the result that the conductor track layers 26 are also completely shielded. A radio-frequency component of this type is consequently protected against electromagnetic interference fields and can be used in many areas, such as preferably as an output stage in mobile radio telephones.

Appellants outlined in the last paragraph on page 25 of the specification, line 25, that Fig. 3 shows a schematic cross section of the electronic component 1 with the shielding 2 according to a third embodiment of the invention. In Fig. 3, components that perform the same function as in the embodiments of Fig. 1 and Fig. 2 are designated by the same reference numerals and an explanation is therefore omitted.

Appellants described on page 26 of the specification, line 6, that, in the embodiment of the invention as shown in Fig. 3, the peripheral annular ground lead 10 has been introduced into the silicon substrate 4 and connected to a peripheral annular solder contact bump. On account of its high impurity concentration, the ground lead 10 is a layer, which has virtually metallic conductivity. Consequently, the active region of the semiconductor chip within the annular highly doped layer is shielded against interference fields.

It is also stated on page 26 of the specification, line 15, that the embodiment of the invention according to Fig. 3 has the advantage that an annular layer at ground potential surrounds the active upper side 5 of the semiconductor chip 3 and at the same time establishes electrical contact for the buried layer 7 in the region of the rear side 6 of the semiconductor chip. The annular solder contact bump is connected via a connecting line 17 in a wiring foil 16 to an external contact bump 28, which for its part is connected via the ground-carrying line 22 to the ground potential terminal 9.

It is outlined in the last paragraph on page 26 of the specification, line 25, that, consequently, the embodiment, which shows the semiconductor chip 3 on the wiring foil 16 and the printed-circuit board 14, on which the electronic component 1 is mounted, is also shielded against stray electromagnetic radiation or interference radiation.

Appellants explained on page 27 of the specification, line 5, that, while the wiring foil 16 is essentially composed of a polyimide, which has a number of conductor track layers of metal, the printed-circuit board 14 is composed of conductor tracks 21 and 22 and also contact vias 29 to 34. In the case

of the embodiment, the wiring foil 16 has the task of increasing the size of the microscopically small, i.e. measurable only with an optical microscope, contact areas 8 of the semiconductor chip 3 to the macroscopic output contact areas 18, which can be perceived and measured with the naked eye, with the result that the macroscopic output contact areas 18 can carry correspondingly visible and adjustable solder contact bumps 20 and the external contact bumps 28 and are matched in their extent to the structures and dimensions of the structures on the printed-circuit board 14.

References Cited:

U.S. Patent No. 4,561,932 (Gris et al.), dated December 31, 1985;

U.S. Patent No. 5,283,454 (Cambou), dated February 1, 1994;

U.S. Patent No. 5,962,924 (Wyland et al.), dated October 5, 1999;

U.S. Patent No. 6,109,530 (Larson et al.), dated August 29, 2000;

U.S. Patent No. 6,317,333 B1 (Baba), dated November 13, 2001.

Issues

1. Whether or not claims 1-3, 5, 6, and 9-12 are obvious over Cambou (U.S. Pat. No. 5,283,454) in view of Baba (U.S. Pat. No. 6,317,333) under 35 U.S.C. § 103(a).

2. Whether or not claim 4 is obvious over Cambou (U.S. Pat. No. 5,283,454) in view of Baba (U.S. Pat. No. 6,317,333) and Gris et al. (U.S. Pat. No. 4,561,932) (hereinafter, "Gris") under 35 U.S.C. § 103(a).

3. Whether or not claim 7 is obvious over Cambou (U.S. Pat. No. 5,283,454) in view of Baba (U.S. Pat. No. 6,317,333) and Wyland et al. (U.S. Pat. No. 5,962,924) (hereinafter, "Wyland") under 35 U.S.C. § 103(a).

4. Whether or not claim 8 is obvious over Cambou (U.S. Pat. No. 5,283,454) in view of Baba (U.S. Pat. No. 6,317,333) and Larson et al. (U.S. Pat. No. 6,109,530) (hereinafter, "Larson") under 35 U.S.C. § 103(a).

Grouping of Claims:

Claim 1 is independent. Claims 2-12 depend on claim 1. The patentability of claims 2, 3, 5, 6, and 9-12 is not separately argued. Therefore, claims 2, 3, 5, 6, and 9-12 stand or fall with claim 1. The patentability of claims 4, 7, and 8 is separately argued and therefore those claims do not stand or fall with claim 1.

Arguments:

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed would be helpful.

Claim 1 calls for, inter alia, an electronic component with **shielding against stray electromagnetic fields**, the electronic component comprising:

at least one ground lead disposed within said semiconductor substrate and having at least one contact area contacting said upper side of said semiconductor substrate for connecting to said ground potential terminal; and

a continuous electrically conductive buried layer having a surface area corresponding in size to said surface area of said passive rear side and entirely extending over said surface area, said buried layer disposed within said semiconductor substrate adjacent said passive rear side and connected to said ground potential terminal through said ground lead for providing a rear side shielding with said buried layer. (emphasis added)

Regarding item 3 on page 2 of the final Office Action, dated March 11, 2003, rejecting claims 1-3, 5, 6, and 9-12 as unpatentable over Cambou (U.S. Pat. No. 5,283,454) in view of Baba (U.S. Pat. No. 6,317,333) under 35 U.S.C. § 103(a), it is noted that the Examiner stated that although "Cambou does not disclose the lead being a ground lead", one of ordinary skill in the art at the time the invention was made would have found it obvious "to ground the lead in Cambou's invention in order to establish a voltage reference for the chip structure." This unsupported conclusory statement is not correct.

The present claimed invention is advantageous in that the active area of the chip is **shielded by the buried layer** (on the rear side of the semiconductor substrate). Sensitivity to stray fields (on the rear side of the semiconductor chip) can be reduced by **shielding** the active area of the chip.

The Cambou reference discloses a semiconductor device having a substrate, a semiconductor device (formed in the substrate) with several electrodes, and a "low sheet resistivity buried layer 14" positioned in the substrate below the semiconductor device (and connecting with one of the electrodes). The buried layer includes a refractory metal. Further, a conductive area is formed in the substrate and is connected

to the buried layer to provide an external connection to the buried layer.

Cambou discloses a semiconductor device 10. The semiconductor device 10 is formed on a substrate 12 (semiconductor wafer) having a buried layer 14 deposited thereon and a semiconductor layer 16 deposited over the buried layer 14. The buried layer has a very low sheet resistivity.

Cambou **does not shield** the chip against stray electromagnetic fields and does not disclose or suggest the need for shielding.

In Fig. 3 of Cambou, the vertical power MOS has three main electrodes, namely, a source electrode 34, a drain electrode 14, and a gate electrode 25 (see Fig. 2). As disclosed in col. 1, lines 12-15, in a conventional vertical power MOS device, the gate and the source electrodes are on the front, or top, major surfaces, and the external drain electrode is on the opposite (bottom or back) major surface.

Thus, Cambou has external contacts on both sides of the substrate, which limits the mounting and applications of such conventional vertical power MOS devices.

Cambou discloses a buried layer 14 in the substrate for contacting the drain electrode so that the external drain contacts are formed on the top major surface. However, in conventional power MOS devices the drain electrode is never grounded, that is, at ground potential. Moreover, the drain electrode is not used for shielding purposes.

Cambou does not disclose that the lead D, the drain electrode, is a ground lead similar to the "buried layer...connected to said ground potential terminal through said ground lead for providing a rear side shielding with said buried layer" as recited in claim 1 of the instant application." Nor has the Examiner shown any motivation, suggestion, or teaching to support his conclusion that it would have been obvious to ground the drain electrode of Cambou's power MOS device in order to provide shielding against stray electromagnetic fields. The features and structural arrangement of claim 1 of the instant application are directed to obtain the claimed **"rear side shielding"** which is not disclosed in Cambou.

In contrast, Cambou merely discloses a buried drain electrode and does not disclose or suggest any sort of shielding as

claimed. Grounding the drain electrode in Cambou would not make any sense.

The secondary reference of Baba does not disclose providing shielding against stray electromagnetic fields according to the present claimed invention. Moreover, Baba does not relate to or disclose the technical problem of providing shielding against stray electromagnetic fields. Accordingly, Baba does not overcome the deficiencies of Cambou, which as discussed above does not disclose shielding of stray electromagnetic fields.

Nor has the Examiner shown sufficient support or justification or motivation in the prior art why one of ordinary skill in the art would even contemplate taking an isolated disclosure of Baba (an external connection 5c to ground) to modify Cambou to ground the lead D.

Clearly, the references do not show "**at least one ground lead disposed within said semiconductor substrate and having at least one contact area contacting said upper side of said semiconductor substrate for connecting to said ground potential terminal; and a continuous electrically conductive buried layer having a surface area corresponding in size to said surface area of said passive rear side and entirely**

extending over said surface area, said buried layer disposed within said semiconductor substrate adjacent said passive rear side and connected to said ground potential terminal through said ground lead for providing a rear side shielding with said buried layer", as recited in claim 1 of the instant application (emphasis added).

Furthermore, in the Advisory Action dated July 1, 2003, the Examiner has stated that the request for reconsideration does not place the instant application in condition for allowance. Specifically, the Examiner has stated that although the references do not explicitly disclose "the shielding against electromagnectic fields", the structure in the primary Cambou reference and the secondary Baba reference "are the same and therefore perform the same function." Moreover, the Examiner stated that it would be obvious to one of ordinary skill in the art at the time of the invention to ground the drain in order to establish a reference potential for the integrated circuit." Appellants submit that the Examiner's statements and conclusions are incorrect and arbitrary without support in the cited prior art. There is absolutely no disclosure or suggestion in the prior art that the proposed combination of Cambou and Baba would result in the claimed feature of shielding against electromagnetic fields as recited in the claim 1. The Examiner's statements are pure conjecture and

wishful thinking in order to find a basis for rejecting the claims. The Examiner's statements are not supported in the prior art and are mere statements of opinion, and as such are insufficient to support the rejection.

It is well settled that almost all claimed inventions are but novel combinations of old features. The courts have held in this context, however, that when "it is necessary to select elements of various teachings in order to form the claimed invention, we ascertain whether there is any suggestion or motivation **in the prior art** to make the selection made by the applicant". Interconnect Planning Corp. v. Feil, 227 USPQ 543, 551 (Fed. Cir. 1985) (emphasis added). "Obviousness can not be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination". In re Bond, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). "Under Section 103 teachings of references can be combined **only** if there is some suggestion or incentive to do so." ACS Hospital Systems, Inc. v. Montefiore Hospital et al., 221 USPQ 929, 933, 732 F.2d 1572 (Fed. Cir. 1984) (emphasis original). "Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be '**clear and particular.**'" Winner Int'l

Royalty Corp. v. Wang, 53 USPQ2d 1580, 1587, 202 F.3d 1340 (Fed. Cir. 2000) (emphasis added; citations omitted); Brown & Williamson Tobacco Corp. v. Philip Morris, Inc., 56 USPQ2d 1456, 1459 (Fed. Cir. Oct. 17, 2000). Appellants believe that there is no "clear and particular" teaching or suggestion in Cambou to incorporate the features of Baba (appellants have pointed out above why one would not consider grounding the drain electrode D of Cambou), or for that matter the features of the other secondary references relied upon by the Examiner.

In establishing a *prima facie* case of obviousness, it is incumbent upon the Examiner to provide a reason why one of ordinary skill in the art would have been led to modify a prior art reference or to combine reference teachings to arrive at the claimed invention. Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Int. 1985). To this end, the requisite motivation must stem from some teaching, suggestion, or inference in the prior art as a whole or from the knowledge generally available to one of ordinary skill in the art and not from the ***applicant's*** disclosure. See, for example, Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1052, 5 USPQ2d 1434, 1439 (Fed. Cir. 1988), *cert. den.*, 488 U.S. 825 (1988). The Examiner has not provided the requisite reason why one of ordinary skill in the art would have been

led to modify Cambou or to combine Cambou's and Baba's teachings to arrive at the claimed invention for providing rear side shielding. Further, the Examiner has not shown the requisite motivation from some teaching, suggestion, or inference in Cambou or Baba or from knowledge available to those skilled in the art.

Appellants respectfully believe that any teaching, suggestion, or incentive possibly derived from the prior art is only present with hindsight judgment in view of the claimed invention. "It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps. The references **themselves** must provide some teaching whereby the applicant's combination would have been obvious." In re Gorman, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991) (emphasis added). In the instant rejection, no such teaching is present in or apparent from the cited prior art references.

Upon evaluation of the Examiner's response and statements, it is respectfully believed that the evidence adduced by the Examiner is insufficient to establish a prima facie case of obviousness with respect to the claims. Accordingly, the

Honorable Board is therefore requested to reverse the final rejection of the Supervisory Primary Examiner.

Regarding item 4 on page 4 of the final Office Action, rejecting claim 4 as unpatentable over Cambou (U.S. Pat. No. 5,283,454) in view of Baba (U.S. Pat. No. 6,317,333) and Gris et al. (U.S. Pat. No. 4,561,932) (hereinafter, "Gris") under 35 U.S.C. § 103(a), it is noted that the Examiner stated that although Cambou and Baba do not disclose "a mono-crystalline silicon substrate", one of ordinary skill in the art at the time of the invention would have found it obvious to use a mono-crystalline substrate to form isolated electronic device components in the substrate. The statement and proposed combination is not correct.

The secondary reference of Gris does not disclose providing shielding against stray electromagnetic fields as recited in the claims. Moreover, Gris does not disclose the technical problem of providing shielding against stray electromagnetic fields. Accordingly, Gris does not overcome the basic deficiencies of Cambou and Baba, neither of which discloses shielding of stray electromagnetic fields.

Nor has the Examiner shown sufficient support or justification in the prior art why one of ordinary skill in

the art would even contemplate taking an isolated disclosure of Gris (a mono-crystalline substrate with dielectrically isolated islets) to modify Cambou to use a mono-crystalline substrate.

The foregoing discussion of Cambou and Baba applies equally in the rejection of claim 4, which depends on claim 1. Gris does not overcome the deficiencies of the Cambou and Baba references individually or in combination.

Regarding item 5 on page 5 of the Office action, rejecting claim 7 as being unpatentable over Cambou (U.S. Pat. No. 5,283,454) in view of Baba (U.S. Pat. No. 6,317,333) and Wyland et al. (U.S. Pat. No. 5,962,924) (hereinafter, "Wyland") under 35 U.S.C. § 103(a), it is noted that the Examiner stated that although Cambou and Baba do not disclose an "electronic component (chip) being a component of a flip-chip mounting technique", one of ordinary skill in the art at the time of the invention would have found it obvious to use the chip of Wyland in Cambou "to increase the circuit density and signal speed." The statement and proposed combination is not correct.

The secondary reference of Wyland does not disclose providing shielding against stray electromagnetic fields as recited in

the instant claims. Moreover, Wyland does not disclose the technical problem of providing shielding against stray electromagnetic fields. Accordingly, Wyland does not overcome the basic deficiencies of Cambou and Baba, neither of which disclose shielding of stray electromagnetic fields.

Nor has the Examiner shown sufficient support or justification in the prior art why one of ordinary skill in the art would even contemplate taking an isolated disclosure of Wyland (flip-chip technology) to modify Cambou to use such technolgy.

The foregoing discussion of Cambou and Baba applies equally in the rejection of claim 4, which depends on claim 1. Wyland does not overcome the deficiencies of the Cambou and Baba references individually or in combination.

Regarding item 6 on page 5 of the final Office Action, rejecting claim 8 as being unpatentable over Cambou (U.S. Pat. No. 5,283,454) in view of Baba (U.S. Pat. No. 6,317,333) and Larson et al. (U.S. Pat. No. 6,109,530) (hereinafter, "Larson") under 35 U.S.C. § 103(a), it is noted that the Examiner stated that although Cambou and Baba do not disclose that the electronic component of claim 1 is "a radio-frequency component", one of ordinary skill in the art at the

time of the invention would have found it obvious to use the chip in Cambou as a radio-frequency component "since chips are used extensively in conventional radio-frequency devices." The statement and proposed combination is not correct. There is no basis whatsoever in the prior art to support the Examiner's conclusory statement.

The secondary reference of Larson does not disclose providing shielding against stray electromagnetic fields according to the present claimed invention. Moreover, Larson does not relate to or disclose the technical problem of providing shielding against stray electromagnetic fields. Accordingly, Larson does not overcome the basic deficiencies of Cambou and Baba, which do not disclose shielding of stray electromagnetic fields.

Nor has the Examiner shown sufficient support or justification in the prior art why one of ordinary skill in the art would even contemplate taking an isolated disclosure of Larson (a radio-frequency chip component) to modify Cambou to use a radio-frequency component.

The foregoing discussion of Cambou and Baba applies equally in the rejection of claim 8 which depends on claim 1. Larson

does not overcome the deficiencies of the Cambou and Baba references individually or in combination.

The Honorable Board is therefore respectfully urged to reverse the final rejection of the Supervisory Primary Examiner.

Respectfully submitted,

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For Appellants

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Appendix - Appealed Claims:

Claim 1 (amended). An electronic component with shielding against stray electromagnetic fields, the electronic component comprising:

a ground potential terminal for receiving an external ground potential;

a semiconductor chip having a semiconductor substrate with an active upper side and a passive rear side having a surface area;

at least one ground lead disposed within said semiconductor substrate and having at least one contact area contacting said upper side of said semiconductor substrate for connecting to said ground potential terminal; and

a continuous electrically conductive buried layer having a surface area corresponding in size to said surface area of said passive rear side and entirely extending over said surface area, said buried layer disposed within said semiconductor substrate adjacent said passive rear side and connected to said ground potential terminal through said ground lead for providing a rear side shielding with said buried layer.

2. The electronic component according to claim 1, wherein said buried layer is formed of a semiconductor material doped with an impurity concentration of over 1×10^{20} cm^{-3}.

3. The electronic component according to claim 2, wherein said semiconductor material is identical to a material forming said semiconductor substrate.

4. The electronic component according to claim 1, wherein said semiconductor substrate is formed of monocrystalline silicon.

5. The electronic component according to claim 1, including an electrically conductive annular layer extending from said upper side of said semiconductor substrate to said buried layer, and disposed in an edge region of said semiconductor chip.

6. The electronic component according to claim 5, wherein said electrically conductive annular layer is formed of a semiconductor material doped with an impurity concentration of over 1×10^{20} cm^{-3}.

7. The electronic component according to claim 1, wherein the electronic component is a component of a flip-chip mounting technique.

8. The electronic component according to claim 1, wherein the electronic component is a radio-frequency component.

9. The electronic component according to claim 1, including solder formations selected from the group consisting of solder balls and solder contact bumps disposed on said contact area.

10. The electronic component according to claim 9, including a mounting device selected from the group consisting of a printed circuit board and a ceramic substrate, and said solder formations mounted to said mounting device.

11. The electronic component according to claim 5, including:

output contact areas;

a wiring foil with connecting lines disposed on said upper side of said semiconductor substrate, said contact area of said semiconductor chip is one of a plurality of contact areas and said connecting lines of said wiring foil connecting said contact area of said semiconductor chip to said output contact areas distributed on said wiring foil; and

solder formation selected from the group consisting of solder balls and solder contact bumps disposed on said output contact areas.

12. The electronic component according to claim 11, wherein said ground potential terminal is connected through at least one of said solder formations, through said wiring foil and through said annular layer to said buried layer.